IDR0224

UNITED STATES PATENT APPLICATION FOR GRANT OF LETTERS PATENT

Mark Moffat
Marcus Granger-Jones
INVENTORS

RECONFIGURABLE FILTER ARCHITECTURE

Withrow & Terranova, P.L.L.C.
P.O. Box 1287
Cary, NC 27512
(919) 654-4520

Docket No. 2867-198

RECONFIGURABLE FILTER ARCHITECTURE

Field of the Invention

[0001] The present invention relates to a reconfigurable filter architecture, and more particularly to a filter architecture having independently configurable gain, bandwidth, and frequency offset.

Background of the Invention

[0002] Multimode receivers are capable of receiving signals according to multiple standards such as the Global System for Mobile Communications (GSM) and Wideband Code-Division-Multiple-Access (WCDMA). In order to accommodate multiple standards, multimode receivers require a variety of different filtering options. In modern receiver architectures, received signals are downcoverted from a radio frequency (RF) to either a very low intermediate frequency (VLIF) or to DC and filtered to remove adjacent channel signals before analog to digital conversion. Filtering at a VLIF requires a filter having a bandpass response, wherein the center frequency of the filter is offset from DC, while filtering at DC requires a filter having a low-pass response. Thus, multimode receivers require separate filters having a passband at DC and at VLIF in order to filter adjacent channel signals before analog to digital conversion. Further, the adjacent channel spacing and widths vary according to standard, thereby requiring filters having varying bandwidths for each standard.

[0003] In order to accommodate the filtering requirements associated with multiple standards, multimode receivers typically include separate filters to accommodate different communication standards. However, these filters require large capacitors that consume valuable chip area. Therefore, there remains a need for a single filter architecture that is easily configurable to accommodate the different requirements of various communications standards.

Summary of the Invention

[0004] The present invention provides a reconfigurable filter having a bandwidth and frequency offset that are independently configured, thereby

allowing the filter to realize any filter pole. In general, the filter includes a filtering stage and a reverse gain stage. The filtering stage has a bandwidth configured by a bandwidth control signal from control logic and a frequency offset configured by an offset control signal. The reverse gain stage provides the offset control signal to the filtering stage based a reverse gain control signal from the control logic and the output signal. Based on the bandwidth control signal and the reverse gain control signal, the bandwidth of the filter is configured independently from the frequency offset of the filter and the frequency offset is configured independently from the bandwidth.

[0005] The filter may also include a forward gain stage that amplifies an input signal to provide the amplified input signal to the filtering stage. A gain of the forward gain stage is configured by a forward gain control signal from the control logic, thereby allowing the gain of the filter to be configured independently from the bandwidth and frequency offset while eliminating the need for additional amplifier stages before the filter.

[0006] Those skilled in the art will appreciate the scope of the present invention and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0007] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the invention, and together with the description serve to explain the principles of the invention.

[0008] Figure 1 is a general block diagram of a system including a reconfigurable filter according to the present invention;

[0009] Figure 2A illustrates configuration of the gain of the reconfigurable filter according to the present invention;

[0010] Figure 2B illustrates configuration of the bandwidth of the reconfigurable filter according to the present invention;

[0011] Figure 2C illustrates configuration of the frequency offset of the reconfigurable filter according to the present invention; and

[0012] Figure 3 illustrates the reconfigurable filter according to one embodiment of the present invention.

Detailed Description of the Preferred Embodiments

[0013] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the invention and illustrate the best mode of practicing the invention. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the invention and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0014] Figure 1 is a general block diagram of a system 10 including control logic 12 and a reconfigurable filter 14, wherein a gain, bandwidth, and frequency offset of the filter 14 are independently configured by the control logic 12. By independently configuring the bandwidth and frequency offset of the filter 14, the filter 14 can be configured to realize any filter pole. In addition, the gain of the filter 14 is configurable without adding additional gain stages.

[0015] In general, the filter 14 includes a forward gain stage 16, a filtering stage 18, and a reverse gain stage 20. The forward gain stage 16 receives an input signal (INPUT) and amplifies the input signal based on a forward gain control signal (FG_CNTL) from the control logic 12. The filtering stage 18 filters the amplified input signal from the gain stage 16 to provide an output signal (OUTPUT). The bandwidth of the filtering stage 18 is configured by a bandwidth control signal (BW_CNTL) from the control logic 12, and the frequency offset of the filtering stage 18 is configured by an offset control signal (OFFSET) from the reverse gain stage 20. The reverse gain stage 20 operates to provide the offset control signal (OFFSET) to the bandwidth stage 18 based on the output signal (OUTPUT) from the filtering stage 18 and a reverse gain control signal (RG_CNTL) from the control logic 12. Each of the forward gain, bandwidth, and reverse gain control signals may be a single control signal or multiple control signals depending on the particular design, as discussed below in more detail.

[0016] Figures 2A-2C illustrate transfer functions of the filter 14 (Figure 1) according to the present invention. Figure 2A illustrates that the configuration of the gain of the filter 14 corresponds to a change in the amplitude of the

transfer function of the filter 14. Figure 2B illustrates that the configuration of the bandwidth of the filter 14 corresponds to a change in the width of the transfer function of the filter 14, and Figure 2C illustrates that the configuration of the frequency offset of the filter 14 corresponds to a shift of the transfer function of the filter 14 from DC (0 Hz). According to the present invention, each of the gain, bandwidth, and frequency offset of the filter 14 are independently configured.

[0017] The transfer functions of Figures 2A-2C correspond to a preferred embodiment of the filter 14, wherein the filter 14 is a fully-complex filter adapted to realize fully-complex filter poles. Since the filter 14 is fully-complex, the filter 14 is capable of distinguishing between positive and negative frequencies. Thus, as is clearly illustrated in Figure 2C, the transfer function of the filter 14 does not include a mirror image response located at a negative frequency.

[0018] Figure 3 illustrates one embodiment of the filter 14 of the present invention, wherein the filter 14 is a first order polyphase filter. In this embodiment, the input and output signals are differential quadrature signals. Accordingly, the input signal includes an in-phase input signal (I_{INPUT}) and a quadrature input signal (Q_{INPUT}), and the output signal includes an in-phase output signal I_{OUTPUT} and a quadrature output signal (Q_{OUTPUT}).

[0019] The forward gain stage 16 includes transistors QF1 and QF2, first and second forward gain resistors REF1 and REF2, and a first current source I1 arranged as shown. The transistors QF1 and QF2 form a first transistor pair that operates to amplify the in-phase input signal (I_{INPUT}) based on the forward gain control signal. In a similar fashion, the forward gain stage 16 also includes transistors QF3 and QF3, third and fourth forward gain resistors REF3 and REF4, and a second current source I2 arranged as shown. The transistors QF3 and QF4 form a second transistor pair that operates to amplify the quadrature input signal (Q_{INPUT}) based on the forward gain control signal.

[0020] The filtering stage 18 receives the amplified in-phase and quadrature input signals from the forward gain stage 16. The filtering stage 18 includes first and second load resistors RL1 and RL2, first and second filtering resistors RF1 and RF2, and a first capacitor C1 arranged as shown and

forming a first filtering circuit that filters the amplified in-phase input signal to provide the in-phase output signal (I_{OUTPUT}). The filtering stage 18 also includes third and fourth load resistors RL3 and RL4, third and fourth filtering resistors RF3 and RF4, and a second capacitor C2 arranged as shown and forming a second filtering circuit that filters the amplified quadrature input signal to provide the quadrature output signal (Q_{OUTPUT}).

[0021] The reverse gain stage 20 includes transistors QR1 and QR2, first and second reverse gain resistors RER1 and RER2, and a third current source I3 arranged as shown. The transistors QR1 and QR2 form a third transistor pair that operates to amplify the in-phase output signal (I_{OUTPUT}) based on the reverse gain control signal (RG_CNTL), thereby providing a first offset control signal (OFFSET1). The reverse gain stage 20 also includes transistors QR3 and QR4, third and fourth reverse gain resistors RER3 and RER4, and a fourth current source I4 arranged as shown. The transistors QR3 and QR4 form a fourth transistor pair that operates to amplify the quadrature output signal (Q_{OUTPUT}) based on the reverse gain control signal (RG_CNTL), thereby providing a second offset control signal (OFFSET2). In one embodiment, the in-phase output signal (I_{OUTPUT}) and the quadrature output signal (Q_{OUTPUT}) that drive the reverse gain stage 20 are essentially ninety degrees out of phase with the in-phase input signal (I_{INPUT}) and the quadrature input signal (Q_{INPUT}), respectively.

[0022] In the embodiment illustrated in Figure 3, each of the resistors REF1-REF4, RF1-RF4, and RER1-RER4 is a variable resistor, each of the load resistors RL1-RL4 is a resistor having a fixed resistance value, and each of the capacitors C1 and C2 is a variable capacitor. The resistance values of the forward gain resistors REF1-REF4 are controlled by the forward gain control signal (FG_CNTL). Optionally, the forward gain control signal (FG_CNTL) may include separate control signals for each of the forward gain resistors REF1-REF4. The resistance values of the resistors RF1-RF4 and the capacitance values of the capacitors C1 and C2 are controlled by the bandwidth control signal (BW_CNTL). The bandwidth control signal (BW_CNTL) of this embodiment may include two control signals each controlling either the filtering resistors RF1-RF4 or the capacitors C1 and C2. Optionally, the bandwidth control signal (BW_CNTL) may include separate

control signals for each of the filtering resistors RF1-RF4 and each of the capacitors C1 and C2. The reverse gain control signal (RG_CNTL) controls the resistance values of the reverse gain resistors RER1-RER4. Optionally, the reverse gain control signal (RG_CNTL) may include separate control signals for each of the reverse gain resistors RER1-RER4. In another embodiment, each of the resistors REF1-REF4 and RER1-RER4 is variable resistor, each of load resistors RL1-RL4 has a fixed resistor value, and the filtering resistors RF1-RF4 and/or the capacitors C1 and C2 are variable.

[0023] One example of a variable resistor is described is U.S. Patent No. 6,552,519 entitled "Variable Impedance Network for an Integrated Circuit", which in incorporated herein by reference in its entirety. One example of a variable capacitor is described in U.S. Patent No. 5,952,952 entitled "Switched-Capacitor Array", which is incorporated herein by reference in its entirety. Many other types of variable resistors and variable capacitors are commonly known in the art and should be considered within the spirit and scope of the present invention.

[0024] As discussed above, the gain, bandwidth, and frequency offset of the filter 14 are independently configurable. Preferably, the forward gain resistors REF1-REF4 have essentially the same resistance value, the load resistors RL1-RL4 have essentially the same resistance value, the filtering resistors RF1-RF4 have essentially the same resistance value, the reverse gain resistors RER1-RER4 have essentially the same resistance value, and the capacitors C1 and C2 have essentially the same capacitance value. Accordingly, the gain of the filter 14 is proportional to the ratio RL1/REF1, the bandwidth of the filter 14 is proportional to C1(RL1+RF1), and the frequency offset of the filter 14 is proportional to RER1. Thus, the gain is configured independently of the bandwidth and frequency offset by controlling the resistance values of the forward gain resistors REF1-REF4. The bandwidth is configured independently of the gain and the frequency offset by controlling the capacitances of the capacitors C1 and C2 and/or the resistance values of the filtering resistors RF1-RF4. The frequency offset is configured independently of the gain and the bandwidth by controlling the resistance of the reverse gain resistors RER1-RER4.

[0025] The filter 14 of the present invention can be configured to realize any filter pole, wherein filter poles take the form X + jY, where X is the bandwidth and Y is the frequency offset. Thus, by independently configuring the bandwidth and frequency offset of the filter 14, as described above, any filter pole can be realized by the filter 14. Further, by cascading multiple filters 14, any complex filter having more than one filter pole can be realized. For example, a fourth order polyphase filter having any four filter poles can be realized by cascading four filters 14, wherein each of the filters 14 is configured to realize one of the four filter poles.

[0026] The filter 14 offers substantial opportunity for variation without departing from the spirit and scope of the present invention. For example, although Figure 3 illustrates one embodiment of a reconfigurable polyphase filter 14, the present invention equally applies to other types of polyphase filters such as the Voorman polyphase filter described in U.S. Patent No. 4,914,408 entitled "Asymmetric Polyphase Filter", which is incorporated herein by reference in its entirety. As another example, the transistor pairs QF1 and QF2, QF3 and QF4, QR1 and QR2, and QR3 and QR4 may be replaced with any number of alternative circuits including but not limited to a CMOS differential pairs, translinear circuits, and operational transconducance amplifiers (OTA's).

[0027] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present invention. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.